Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An integrated memory, comprising:

a plurality of memory cells in a memory cell array, the memory cells being combined to form individually addressable normal units;

a plurality of redundant units of memory cells for respectively replacing one of the normal units on an address basis;

a memory unit for storing, in a normal mode, an address for one of the normal units which needs to be replaced by one of the redundant units;

a comparison unit~~, the comparison unit being~~ connected to an address bus in the memory and to an output of the memory unit ~~for the purpose of~~ , the comparison unit comparing an address which is present on the address bus with an address stored in the memory unit and ~~for the purpose of~~ activating one of the redundant units in the event of a match being identified; and

a test circuit~~, the test circuit being~~ activated by a test mode signal[[,]] and ~~the test circuit adapted~~ operable to reset the memory unit to an initial state and to store an ~~address~~ identification code for one of the redundant units in the memory unit for subsequently writing the identification code to the ~~redundant unit~~ one of the redundant units, wherein the identification code represents a position of the one of the redundant units in the memory cell array, and each of the redundant units is discriminated by a respective identification code.

2. (Currently Amended) The integrated memory as claimed in claim 1, wherein the memory unit is programmable, and the memory ~~has~~ includes a second nonvolatile memory unit for permanently storing an address~~, the memory further having~~ and ~~has~~ at least one output which

is connected to a corresponding input of the memory unit for transmitting an address stored in the second memory unit to the programmable memory unit.

3. (Original) The integrated memory as claimed in claim 2, wherein the second nonvolatile memory unit can be programmed only once.

4. (Original) The integrated memory as claimed in claim 2, wherein the second nonvolatile memory unit has laser fuses, which can be programmed from outside the memory by a laser beam.

5. (Original) The integrated memory as claimed in claim 1, wherein the memory is in the form of a DRAM.

6. (Original) The integrated memory as claimed in claim 1, wherein the memory unit is in the form of a register having register elements for storing a respective address bit.

7. (Currently Amended) A method for testing an integrated memory~~, the integrated memory having~~ including a plurality of memory cells in a memory cell array, the memory cells being combined to form individually addressable normal units, a plurality of redundant units of memory cells for respectively replacing one of the normal units on an address basis, a memory unit for storing, in a normal mode, an address for one of the normal units which needs to be replaced by one of the redundant units, a comparison unit which is connected to an address bus in the memory and to an output of the memory unit for comparing an address which is present on the address bus with an address stored in the memory unit and for activating one of the redundant units in the event of a match being identified, the method comprising:

activating a test mode;

resetting the memory unit to an initial state;

storing an ~~address~~ identification code for one of the redundant units in the memory unit, wherein the identification code represents a position of the one of the redundant units in the memory cell array, and each of the redundant units is discriminated by a respective identification code;

writing ~~an~~ the identification code to the one of the redundant units;

deactivating the test mode;

setting the memory unit using the address for one of the normal units which needs to be replaced;

accessing the memory cell array;

applying addresses for normal units to the address bus for reading the memory cell array;

reading the memory cell array; and

associating the identification code which is read with the address for the normal unit addressed for this reading operation.